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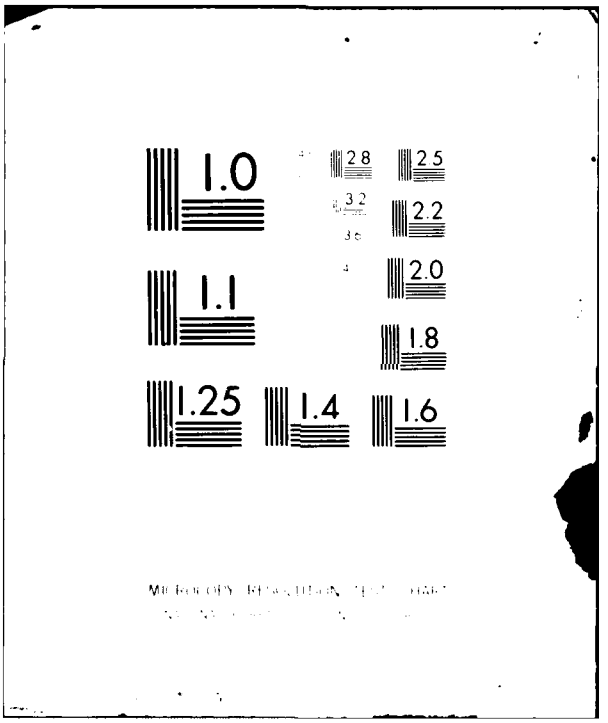
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IMAGE PROCESSING DISPLAYS: A REPORT ON COMMERCIALLY AVAILABLE STATE-OF-THE-ART FEATURES

R. LaPado
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IMAGE PROCESSING DISPLAYS: A REPORT ON COMMERCIALLY AVAILABLE STATE-OF-THE-ART FEATURES

1. INTRODUCTION.

This report summarizes an in-house study conducted by ESL Incorporated on the state-of-the-art of Digital Image Processing Display Technology. The purpose of the study was to determine the level of technology, maintenance support and subsequent cost that could be expected from the display vendor community in the near term (6 months). The study was directed at the evaluation of real-time color digital image display systems having multiple refresh memory, multiple graphics display, interactive capability and full color operation using a 512 x 512 element image array.

The display evaluation was conducted over a 6 month period. It entailed an in-depth literature search, a study of system brochures, interviews with vendor management and technical staff and demonstrations of display operations. Additionally, each of the vendor companies was evaluated on financial stability, production record, field support performance and technical expertise. Based on the evaluation, 10 vendors were identified as potential suppliers with sufficient technical strength and stability to incorporate the display features that would be required on a state-of-the-art display system. The 10 vendors in alphabetical order are:

- Aydin
- Comtal
- DeAnza
- Genisco
- Grinnell

1. -- Continued.

- Hazeltine
- I^2S
- ISI
- Lexidata
- Ramtek

Although the display features offered by these vendors vary considerably in sophistication, the basic functional capabilities of the systems can be grouped generically to permit each vendor's display to be evaluated on particular functional characteristics. The actual display evaluation was conducted on the system design and functional capabilities incorporated in the top-of-the-line display unit produced by each of the vendors and revealed that no one display system incorporated all of the features available on the others. This can be partly attributed to the small company nature of all of the vendors and the fact that these display systems were each developed for particular image processing applications.

The basic functional requirements against which the display systems were to be evaluated, were initially established to be equivalent to the present capabilities of the ESL IDIMS display. Early in the study, however, it became apparent that additional functional capabilities were common to several of the display systems with no apparent impact on cost. These capabilities and the basic system requirements now constitute what are termed in this report, the mandatory display system requirements.

It was noted that several of the display systems incorporated unique features that would greatly enhance the performance of an image processing display and should be incorporated if the cost impact were not prohibitive. These features were combined to produce a list of what are termed in this report, desirable display system requirements.

1. -- Continued.

All of the features, both mandatory and desirable, should be considered to be within or at the present state-of-the-art in display technology and should not generate an unbearable amount of nonrecurring engineering cost by their required inclusion in a display system.

This report covers the general design of image display systems, a detailed analysis of commercially available display features and recommendations for the design and configuration of a state-of-the-art image processing display.

2. DISPLAY SYSTEMS ARCHITECTURES.

The earliest real time image displays were designed almost exclusively around the single problem of handling the high refresh data rate. As such, the designs were very simple and since they used a disk for refresh, they had hardwired data paths from the host interface, through the disk, a set of lookup tables, the DACs and to the monitor. The implementation of RAM refresh memories and the steady advances in logic speeds have since allowed more flexibility in design and true systems design has recently been applied, with resultant improvements in modularity, flexibility and programmability.

Although each display system manufacturer has a unique design, several classes of system can be identified and will be discussed here. It is worth noting that individual designs are best suited to certain applications -- multispectral data analysis is facilitated by the multiple refresh channel and highly parallel, sophisticated color combination capabilities of the I^2S Model 70 display, while detailed analysis of reconnaissance imagery is greatly aided by the sophisticated interactive processing capabilities of the DeAnza Systems IP5000 series display.

The early display designs have tended to evolve to include a microprocessor as shown in Figure 2-1. Multiple refresh memories and graphics overlays are available with black and white and pseudo-color lookup tables. The displays manufactured by Genisco, COMTAL, Lexidata, and Ramtek follow this basic design philosophy. The Grinnell and Hazeltine displays are of this form but without internal intelligence. In some systems (e.g., Lexidata) the microprocessor solely performs system control. In this case, the data flow is basically a single direction, from interface to monitor. In other cases (e.g., Genisco), the microprocessor is complemented with processing memory and the display system can implement image processing algorithms by fetching data from refresh. Such processing is, of course, fairly slow, being

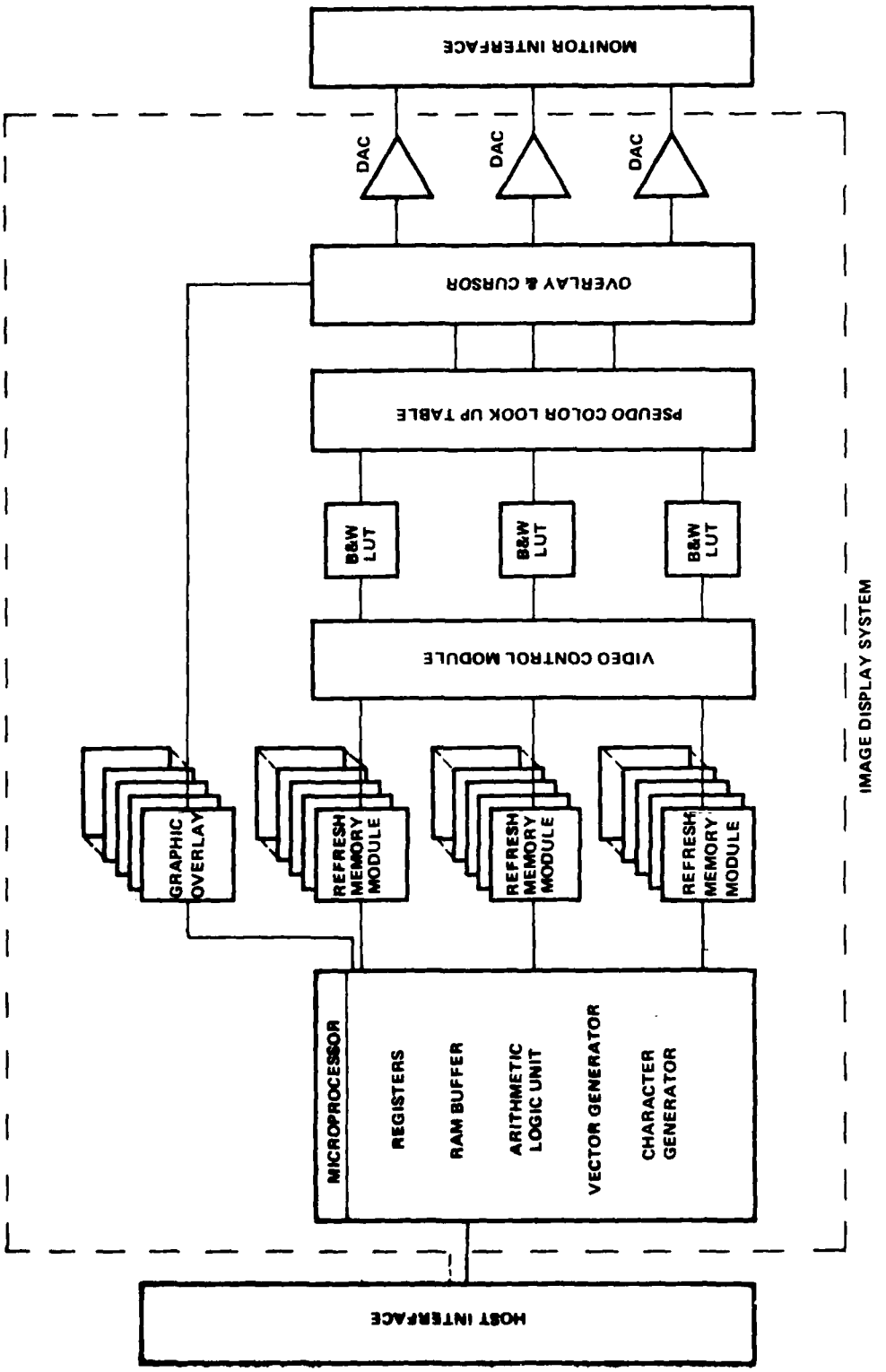


Figure 2-1. Top Level System Block Diagram (Microprocessor Architecture)

2. -- Continued.

limited both by the data I/O between microprocessor memory and refresh memory and by the limited capabilities of the microprocessor.

The products released in 1978 by Aydin and ISI exhibit a bus oriented architecture, an example of which is shown in Figure 2-2. Currently it is beyond the state-of-the-art to implement a refresh bus, so there are still hardwired lines from refresh to display, however, for control and internal processing, all subsystems are bus connected. Obvious advantages include flexibility and modularity: allowing for growth in both capability and size. Processing can be performed by shuttling data between memory and the processor as with the first design, but in addition, the memory bus allows manipulation of data between refresh memories. As a result, operations such as connecting subsegments of one image into another, scrolling and split-screening are easily performed.

The third architecture -- feedback loop illustrated in Figure 2-3 -- is oriented to performing very rapid image processing. The general features of black and white and color lookup, vector generation, overlays, etc. are all provided, but the refresh memories are interconnected via a very high speed (refresh rate) processor. The best example of this architecture is DeAnza Systems IP5000 series display, where any refresh memory can be selected for input or output and two memories may be connected on both input and output such that 16 bit arithmetic precision may be maintained. A feedback loop of limited precision and capability is available on the I^2S and Hazeltine displays. The feedback loop concept is successful for image processing for two reasons:

a. The data handling problem is solved by direct interfacing to the large refresh memory data base at real-time video rates.

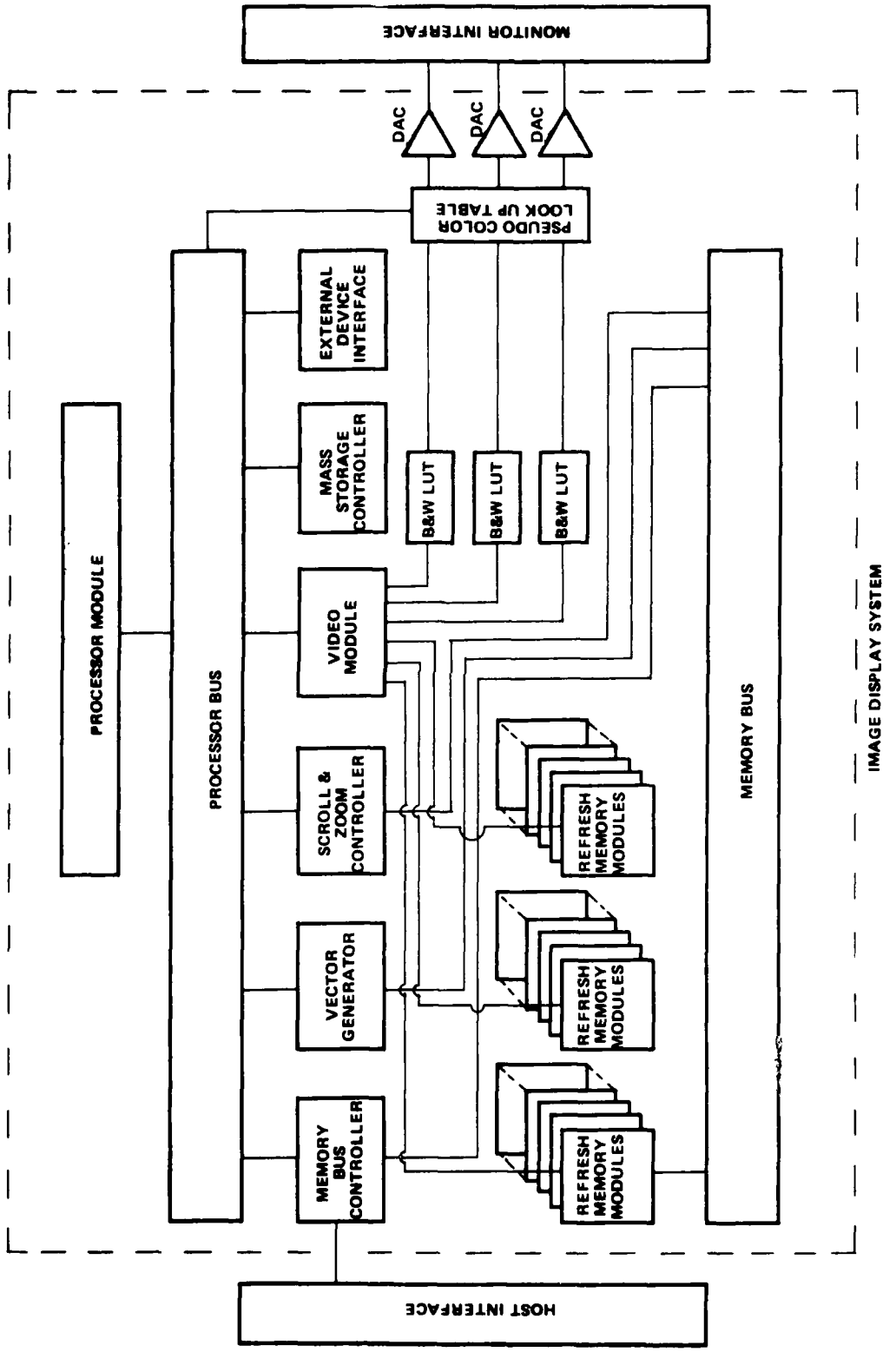


Figure 2-2. Top Level System Block Diagram (Bus Architecture)

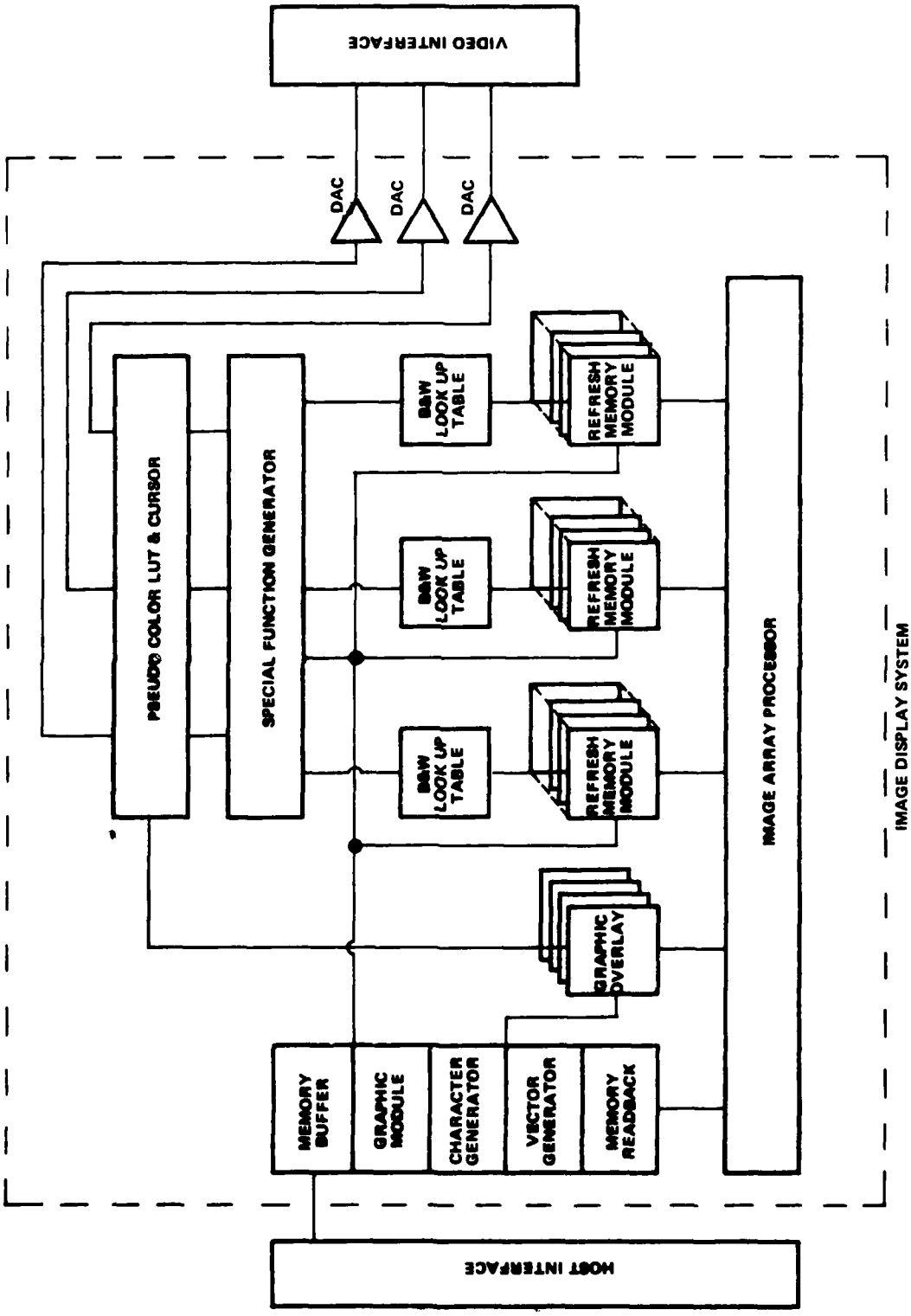


Figure 2-3. Top Level System Block Diagram (Feedback Loop Architecture)

2. -- Continued.

b. The computation problem is tackled by pipelining simple arithmetic and logical operations in the image array processor.

This processing approach is successful becomes most image processing algorithms can be reduced to an iteration of those simple operations. For example, convolutions with modest size kernals can be performed within seconds.

The distinctions between the three example architectures are not absolute (the DeAnza Systems display incorporates a microprocessor as well as the feedback loop). As display technology matures, it is expected that designs will standardize, probably being bus oriented but incorporating feedback processing and internal intelligence. Some advanced capabilities are worthy of special note. DeAnza produces a system called Visicom in which refresh memory is configured as a single channel but of greater depth (currently 16 bits) and is interfaced with an internal microprocessor (LSI-11) to look like main memory to that processor. Lexidata systems have refresh memory which under program control can refresh screens in different formats (512 x 512 pixel, 512 x 640 pixel, 30 frames/second of 2:1 interlace or 60 frames/second, no interface). The ISI system has refresh which consists of a single, very long vector but which is programmably configurable to handle images of various sizes for display in various formats.

3. DISPLAY SYSTEM CHARACTERISTICS.

In order to facilitate an objective evaluation of the functional capabilities of the display systems produced by the vendors identified in the Introduction of this report, 20 image processing display system attributes were selected to be the basis of the technical evaluation. These attributes are:

- Refresh Memory
- Graphics Overlay
- Look-up Tables (B&W)
- Look-up Tables (Color)
- Interactive Controls
- Cursor
- Programmable Switches
- Readback Link
- Test Patterns
- D/A Converters
- Scroll
- Zoom
- Histogram
- Split Screen
- Vector Generator
- Character Generator
- Image Combination
- Feedback Loop
- Microprocessor
- Interfaces

This section will separately treat each of these attributes by defining the term, describing its physical and functional characteristics, operation and implementation techniques observed in the evaluated systems. Each section will be followed by a matrix containing the features that relate to each attribute by vendor.

3. -- Continued.

The vendors are listed in alphabetical order and the data contained in each matrix is based on latest information made available to ESL.

3.1 Refresh Memory.

The refresh memory allows the image display system to operate without host CPU interaction during operations that require no image update. These memories are initially loaded by the host computer. Once loaded, the refresh memory is accessed internally by the display electronics to provide a continuous stream of image data to the digital-to-analog converters (DACs) for display on a video monitor.

Today, refresh memory is constructed from one of three types of solid-state technology:

- Random Access Memory (Dynamic)
- Random Access Memory (Static)
- Charge Coupled Device Memory

Both Dynamic and Static Random Access Memories (RAMs) are available with 4K or 16K bits per chip density (some manufacturers are now producing limited quantities of 64K bit chips). The Charge Coupled Device (CCD) memories are available in both 16K and 64K bit densities (with up to 256K bit density in limited quantities).

The RAM and CCD refresh have the following features:

- STATIC RAM
  - Asynchronous data access (addressable)
  - No refresh needed to maintain data

3.1 -- Continued.

- More power required than the dynamic RAM
- Tends to be faster
- Most expensive

- DYNAMIC RAM
  - Asynchronous data access (addressable)
  - Decay time of 2 msec per bit
  - Low power requirement
  - Less expensive than STATIC RAM

- CCD MEMORY
  - Requires synchronous data access
  - Higher density components available
  - Least expensive components
  - Slowest interactive access to data.

The refresh memories are typically assembled from groups of memory cards, each of which contains sufficient storage for one or two bit planes. (A bit plane contains storage for a 512 x 512 x 1 array of data.) When these bit planes are electronically stacked, commonly in groups of 8, they can store and refresh an entire image with 256 intensity values for each pixel. This group of refresh memory is termed an image plane and is used to store and refresh one channel (Red, Green, Blue or Black and White) of image data. Three of these image plane modules must be used simultaneously to refresh a full color video image.

The rates at which the video refresh occurs (either 30 or 60 frames per second) are much higher than the refresh memory can operate. Therefore, it is a common technique to access 8 or 16 pixels in parallel through a multiplexing circuit (each channel having its own controller) to increase the refresh rate through the DACs to match the video raster rate.

3.1 -- Continued.

Several display systems provide microprocessor control to yield advanced capabilities over the more basic refresh architectures. The microprocessors enable the display system to aggregate two or more image planes to provide increased intensity representations of an image. Additionally, these microprogrammable displays can associate four image planes so the image area is increased from 512 x 512 to 1024 x 1024 using one image plane for each of four quadrants. This enables an analyst to zoom or pan through the extended image without having the host CPU rewrite a composite image to an additional image plane memory.

The amount of image refresh memories available on existing systems varies between 3 and 12 image planes.

Most of the display system RAM refresh memories are dual-ported, allowing simultaneous, asynchronous refresh and host computer or internal processor access. This feature provides efficient interactive access of display data for processing or loading functions, independent of refresh operations.

A less flexible alternate architecture is called module interleaving. In this configuration each memory is broken into independent modules, only one of which, at any instant is being used for refresh. This scheme allows processor access to all but a small portion of an image at any one time and guarantees that all pixels of an image will be accessable at some time during each refresh cycle.

The shift register nature of CCD memories precludes asynchronous computer access. Independent processing access ports can be provided for the memories, but of course are subject to the same latency and serial access constraints as the refresh.

3.1 -- Continued.

A future trend in refresh memory architecture which is currently available on at least one system is a fully programmable refresh where the refresh memory size and organizations can be reconfigured under microprocessor control, in much the same way as main memory is dynamically allocated in a general purpose computer.

Refresh Memory Basic Requirements and Desirable Features.

3.1.1 Basic Requirement.

The following is a list of basic refresh memory characteristics that should be required on a new image processing display system:

Size:	512 x 512 pixels
Depth:	8 bits (minimum)
Number:	up to 12
Type:	RAM
Access:	Dual ported or module interleaved
Load Rate:	Any desired pixel in $\leq$1.5 μs

3.1.2 Desirable Feature.

The following additional requirements are listed in decreasing order of desirability:

Programmably Reconfigurable Refresh Memory Format.

a. Refresh of 1024 x 1024 pixel display (8 bits per pixel) [probably effected by loading the image into four 512 x 512 pixel (8 bits per pixel) memories].

3.1.2 -- Continued.

b. Refresh of 512 x 512 pixel (8 bits per pixel) display from any 512 x 512 pixel sub-array of a 1024 x 1024 pixel image. Effected by loading the image into four 512 x 512 pixel memories and suitable manipulation of scrolling and split-screen capabilities.

c. Programmable selection of refresh at 512 x 512 pixels, 30 frames per second, 2:1 interlace or at 512 x 512 pixels, 60 frames per second, no interlace.

d. Refresh of 512 x 512 pixels at greater than 8, less than or equal to 16 bits per pixel. Probably effected by loading two 512 x 512 pixel (8 bits per pixel) refresh memories with the data and mapping down to 8 bits per pixel for display with a higher input precision look-up table. Practical considerations probably limit this to 12 bit input (4096 word size) but these 12 bits should be selectable from the full 16 bits if such are provided.

REFRESH MEMORIES

FEATURE / DISPLAY	TYPE	NUMBER OF RFMS	SIZE IN PIXEL	DEPTH IN BITS	ASSOCIATION FOR AREA INCREASE	ASSOCIATION FOR DEPTH INCREASE	DUAL PORTED					
AYDIN	4K OR 16K RAM	16	PROG.	PROG.	YES	YES	YES					
COMTAL	4K OR 16K RAM	6	512 x 512	8	NO	NO	YES					
DE ANZA	16K RAM	4	512 x 512	8	YES	YES	YES					
GENISCO	16K RAM	4	512 x 512	8	NO	NO	YES					
GRINNELL	4K RAM	3	512 x 512	8	NO	NO	NO					
HAZELTINE	16K RAM	10	512 x 512	8	YES	NO	YES					
ISI	4K STATIC RAM	PROG.	PROG.	PROG.	YES	YES	NO					
I^2S	4K RAM	12	512 x 512	8	YES	YES	YES					
LEXIDATA	4K RAM	>6	512 x 512	8	YES	YES	YES					
RAMTEK	16K RAM	6	512 x 512	16	YES	YES	YES					

3.2 Graphics Overlays.

Graphics overlays are commonly single bit image planes used to merge line and character data with display images. These binary images are generally constructed by the display system operator to annotate processed image data, or to display graphs of image related statistical data.

The generated graphics data are stored in the same type of memory as the image refresh, (RAM or CCD) and have the same monitor and host computer access characteristics.

The graphics overlays are usually generated by interactive input devices such as those listed below:

- ASCII KEYBOARD
- X-Y GRAPHIC TABLET
- TRACKBALL
- JOYSTICK

These devices drive the character generator and vector generator modules that are part of the display system electronics. The number of bit planes assigned to graphics currently ranges from two to 16 with color display of graphics available on all systems. There are presently four methods of combining overlay data with display images:

- REPLACEMENT - replaces all pixels of image data, coincident with even valued graphics data, with pre-assigned intensities while graphics are on.

- COMBINATION - performs a logical AND operation between the graphics and the display image to generate a new image with the graphics embedded.

3.2 -- Continued.

- LOOKUP TABLE - combines graphics and image data through a pre-set of intensity assignments while graphics are on.

- MOST SIGNIFICANT BIT (MSB) FLIP - reverses the most significant bit in every pixel that is coincident with an even valued graphics pixel.

- HIERARCHICAL OVERRIDE - a programmable hierarchy is established to result in successive override of lower priority overlays where the cursor always has top priority.

The color display of graphics is accomplished through binary (on/off) assignments to the monitor color guns. This results in eight possible colors including black and white.

Graphics Overlay Basic Requirements and Desirable Features.

3.2.1 Basic Requirement.

The following is a list of basic graphics overlay characteristics that should be required on a new image processing display system:

Size:	512 x 512 pixels
Depth:	1 bit
Number:	up to 4
Type:	RAM
Access:	Dual ported or module interleaved
Load Rate:	16 consecutive pixels in $\leq$3.0 μs

3.2.1 -- Continued.

Colors:	8 (inc. black and white)
Method of Combination with Imagery:	Programmable between three options: Replacement, Summation, Color Contrast
Method of Combining Multiple Graphics:	Programmable between two options: Color Combination, Hierarchical Override

3.2.2 Desirable Features.

A desirable feature of the graphics overlay is independent scrolling. This feature would allow an operator to pan an overlay(s) up and down on left and right across an image on the display.

GRAPHICS OVERLAYS

FEATURE / DISPLAY	TYPE	NUMBER OF OVERLAYS	SIZE IN PIXELS	METHOD OF COMBINATION	COLOR	INDEPENDENT SCROLLING						
AYDIN	4K OR 16K RAM	VARIABLE	VARIABLE	REPLACE & COMBINE	YES	YES						
COMTAL	4K OR 16K RAM	4	512 x 512	REPLACE & COMBINE	YES	NO						
DE ANZA	16K RAM	8	512 x 512	CONTRAST &REPLACE & COMBINE	YES	ALL AT ONCE						
GENISCO	16K RAM	4	512 x 512	REPLACE OR THRU LUT	YES	YES						
GRINNELL	4K RAM	3	512 x 512	REPLACE	YES	YES						
HAZELTINE	16K RAM	8	512 x 512	REPLACE OR MSB FLIP	YES	YES						
ISI	4K STATIC RAM	2	512 x 512	THRU LUT	YES	??						
I^2S	4K RAM	8	512 x 512	REPLACE & COMBINE	YES	ALL AT ONCE						
LEXIDATA	4K OR 16K RAM	8	512 x 512	PROG. PROM	YES	YES						
RAMTEK	16K RAM	16	512 x 512	THRU LUT OR REPLACE	YES	YES						

3.3 Black and White Look-up Tables.

Black and white look-up tables (LUTs) are used to apply intensity transformations to the image data read from the display refresh memories. The LUT mapping is accomplished by using programmable random access memory, (RAM), and by allowing the tabled transformation to be modified according to the input/output requirements. Each refresh memory is usually configured with its own look-up table. This facilitates the high data rate requirement imposed by the video monitor.

The look-up tables have two common applications.

a. The LUT is used when the intensity range of the image data exceeds 8-bits (256 levels) which is a common input requirement for the D/A converters. The excess intensity range often occurs following the application of various arithmetic or image combination functions. The re-scaling is required to maintain the full range of image data through the system to the display monitor.

b. The look-up tables can be loaded to perform non-linear image enhancement functions. (i.e., logarithmic, radiometric, exponentiation). These functions can be accomplished by re-loading the RAM look-up table from tables stored in the host system.

The look-up table RAM is a two-dimensional array with one dimension being equivalent to the output intensity range of the refresh memory, and the other dimension is equal to the output range of the LUT. As each pixel is read out of the refresh memory, its bit level

3.3 -- Continued.

value is determined and used to address the input of the LUT. The value in the table at that address is then used to replace the old pixel value. This procedure allows the transformed image to be displayed without modifying the original image stored in the refresh memory.

The look-up table feature is common in most display systems, with some vendors providing up to six different look-up table memories in a single display.

Black and White Look-Up Table Basic Requirements and Desirable Features.

3.3.1 Basic Requirements.

The following is a list of the basic black and white look-up table characteristics that should be incorporated in a new image processing image display system:

Number:	One per refresh memory
Size:	256 8-bit words (minimum)
Input Width:	8 bits (minimum)
Output Width:	8 bits (minimum)
Load Synch:	Loadable only during vertical retrace period
Load Time:	Fully loadable during vertical retrace period
Interference:	No noise on video during load, no interference with video synch

3.3.2 Desirable Features.

It would be desirable to have the capability of accessing a graphical presentation of the look-up table function by means of direct control over the vector generator module. The graph of the functions should be displayed using the full display screen.

BLACK & WHITE LOOK UP TABLES

FEATURE / DISPLAY	#	INPUT: BIT WIDTH	OUTPUT: BIT WIDTH	LOADABLE DURING VERTICAL RETRACE								
AYDIN	>4	12	12	??								
COMTAL	3	8	8	YES								
DE ANZA	1	8	8	YES								
GENISCO	3	8/12	8/6	YES								
GRINNELL	3	8	8	YES								
HAZELTINE	5	8	8	YES								
ISI	4	8	16	NO								
I^2S	1 INPUT 3 LUT/RFM 3 OUTPUT FUNC MEMORY	12 (13 OPT) 8 13	8 8(+SIGN) 10	YES								
LEXIDATA	ONE PER REFRESH	≤14	4x8	NO								
RAMTEK	6	12	8	YES								

3.4 Color Look-up Tables.

The color look-up tables serve two functions:

a. True color and false color scaling
b. Pseudo-color scaling.

The true color and false color look-up tables operates exactly as the black and white look-up tables except that there are three LUTs in operation in the color table (one for each of the color channels). In the true color mode, three channels of data from the red, green and blue assigned refresh memories operate in parallel through the display system. The color LUT performs a linear mapping on the data to produce a data stream compatible with the corresponding red, green and blue D/A converters (DACs). The data is then passed in video form to the red, green and blue color guns in the video monitor resulting in a true or normal color image. The false color term is used when the data channels are imaged through different color guns (i.e., green on red, blue on green and red on blue). The full dynamic range of the D/A converters is used (typically, 8-bit) in both the true color and false color modes.

The pseudo-color LUT differs from the true color LUT in that it is a serial-to-parallel stream from only one image channel. In this mode each pixel value in the original image (single channel) is mapped to three separate, typically 4-bit values (one for each channel in the color monitor). The ratio of these three values determines the resultant color of the pixel on the monitor. This scheme provides up to 4096 different color assignments.

3.4 -- Continued.

The color LUT operates the same as the black and white LUT in that the input pixel value determines the address in the table and the output is the transformed value. In the pseudo-color mode the pseudo-color table is a 1 x 3 array where the input pixel value is the LUT input address to three bins each of which outputs a pre-loaded value to its respective color channel. Although these configurations are adequate for most display operations, the configuration flexibility of the PROM LUTs make it a simple matter for vendors to offer options for inputting up to 24-bit data and outputting up to 14-bits of intensity to each channel of the color video monitor.

Color Look-Up Table Basic Requirements.

The following is a list of the basic color look-up table characteristics that should be incorporated on a state-of-the-art image processing display system.

Pseudo-Color LUT.

Size:	256 12-bit words (minimum)
Input Width:	8 bits (minimum)
Output Width:	3 x 4 bits (minimum)
Load Synch:	Loadable only during vertical retrace period
Load Time:	Fully loadable during vertical retrace period
Interference:	No noise on video during load, no interference with video sync

True and False Color.

Precision:	8 bits per color

PSEUDO-COLOR LUT'S & TRUE COLOR

FEATURE / DISPLAY	INPUT SIZE IN BITS	OUTPUT SIZE IN BITS/COLOR	INDEPENDENTLY SELECTABLE	TRUE COLOR NUMBER OF BITS/COLOR								
AYDIN	8	8	YES	8								
COMTAL	6 OR 8	4 OR 8	YES	8								
DE ANZA	8	4	YES	8								
GENISCO	8	4	YES	8								
GRINNELL	8	8	YES	8								
HAZELTINE	8	8	YES	8								
ISI	16	14	NO	0								
I^2S	8	10	YES	10								
LEXIDATA	10	8	YES	8								
RAMTEK	8	8	YES	8								

3.5 Interactive Input Devices (Trackball, Position Joystick, and Rate Joystick).

The trackball, position joystick, and rate joystick are interactive peripheral devices used by the image display system operator to position a cursor at a predetermined location on the display screen. All of these devices are interfaced directly to the image display system and use a serial transmission signal to drive the cursor from one X,Y address to another. Each of the devices can be equipped with several function buttons that are capable of transmitting an interrupt signal to the host computer in order to, for example, change the status of the device operation. The manual positioning of the cursor with these devices serves three basic functions:

a. Visual flagging of a pixel or area of interest on the displayed image

b. Locating a specific pixel from which data is to be read to the display processor or host CPU

c. Positioning the cursor at a desired numerical X,Y position (using the row/column pixel matrix to represent cartesian coordinates) to define independent variables in a two-dimensional function. This is commonly used for various image intensity transformations.

The trackball, position joystick, and rate joystick differ in the following way:

a. The trackball and position joystick are position control devices

b. the rate joystick is a directional rate device.

3.5 -- Continued.

The trackball is operated by rotating a free spinning captured sphere. At rest, the device is continuously transmitting a fixed coordinate pair. When the sphere is rotated in the socket, the coordinates increase or decrease serially until the rotation stops. The direction of spin determines whether the coordinate address in X and Y increase or decrease. The sphere can be spun at any angle causing the cursor to move at a similar angle at a rate proportional to the rate of spin.

The position joystick is operated by pressing the joystick (or lever) in the direction that the pixel is to be moved on the display. When the joystick is straight up, the cursor is positioned in the center of the display image. As the joystick is moved forward, the cursor moves up. When released, the lever does not return and each angle of the joystick represents a position for the cursor in the image. Therefore, when the joystick is placed in a constant non-vertical position, the cursor remains fixed at a point away from the center of the display image.

The rate joystick is operated by moving the lever in any direction from the center (at rest) position. This causes the cursor to move in the same direction on the display. The more the joystick is pressed, the faster the cursor moves in the same direction. When the joystick is held in a constant position (away from rest) the cursor moves at a constant rate across the display. Release of the joystick returns it to the spring loaded position and stops the cursor movement, leaving it at the current screen location.

There are three ways in whic the trackball, position joystick, and rate joystick can control the cursor position:

3.5 -- Continued.

a. Host CPU software control
b. Internal Display microprocessor control
c. Direct hardwire link to display.

In all three interfacing techniques the output of the device is a constant transmission signal. This signal can either be polled by the receiving unit, which involves a periodic check of the signal to update the device status or cursor position, or, the device can operate in a mode where the device transmits an interrupt to the controlling unit whenever new data is being transmitted.

Interactive Input Device Basic Requirements.

The following is a list of basic requirements for interactive input devices that should be incorporated on a new image processing system display:

Trackball:	Digital accuracy and noise level such that less than 1 pixel* jitter is achieved when controlling a cursor. *1 pixel of a 1024 x 1024 pixel display.
Rate Joystick:	8 bit digital accuracy
Function Buttons:	4 (minimum) on trackball and joystick assemblies
Interrupts:	All interactive devices shall be capable of interrupting the host

INTERACTIVE INPUTS

FEATURE / DISPLAY	TRACKBALL	JOYSTICK RATE	JOYSTICK POSITION	GRAPHICS TABLET	NUMBER OF FUNCTION BUTTONS	INTERRUPT GENERATION						
AYDIN	YES	YES	NO	YES	0	N/A						
COMTAL	YES	NO	NO	YES	0	N/A						
DE ANZA	YES	YES (SWITCHABLE)	YES (SWITCHABLE)	OPT.	5	YES						
GENISCO	YES	YES	NO	YES	8	YES						
GRINNELL	YES	YES	NO	NO	4	??						
HAZELTINE	NO	YES	YES	NO	36	YES						
ISI	YES	NO	NO	NO	43	YES						
I^2S	YES	NO	NO	NO	4	YES						
LEXIDATA	YES	YES	NO	THINKING ABOUT IT	8	NO						
RAMTEK	YES	YES	YES	YES	4	YES						

3.6 Cursors.

A cursor is a small target on an image display. Used interactively, it provides a visual reference of an X,Y address in a digital image array. The cursor can be positioned on any pixel in a displayed image by using one of several interactive devices (track-ball, joystick light pen, etc.). The location of the cursor defines a pixel coordinate that can be used by the display system or host computer to access specific pixel intensity data or define a subset of the displayed image. The coordinate data acquired in this manner may then be used to access pixel data for processing functions or to generate spatial limits for subsequent display operations.

There are three types of cursors available on display systems:

a. Fixed cursors
b. Window cursors
c. Programmable cursors.

The fixed cursors are pre-set in a fixed pattern. Although there are usually options as to their shape, once the selection has been made it is not modifiable. Many vendors offer systems with a number of fixed cursors under selector switch control. This enables an operator to select a cursor based on the properties of the image being viewed. Fixed cursors generally take the form of dots, crosses, characters, full screen crosshairs or dashed lines. These patterns are generated to allow the operator to facilitate locating a single pixel.

The window cursor is used to specify a rectangular area in the display image. Its shape, although always rectangular, can be

3.6 -- Continued.

changed by the operator to outline any number of rows or columns of pixel data. This type of cursor is commonly used to identify sub-sections of a display image for special processing.

Programmable cursors are provided with many of the available display systems. In these systems, a cursor array is allocated for overlay display under trackball or joystick control. The size of the array varies by vendor but ranges from 10 x 10 to 64 x 64 pixels. The content of the cursor array is programmable from the host computer (or internal microprocessor if provided) allowing the operator to generate the size and shape of the cursor.

The primary requirement of the cursor is that it be visually discernable against the image background. This is accomplished by attempting to produce a contrast between the cursor and the image surrounding the cursor position. In order to enhance the detectability of the cursor many vendors offer features such as cursor blinking, color cursors and cursors controlled by intensity transformation functions.

The display of the cursor is accomplished in the same manner as the graphics overlay in that at a given position the background image is temporarily modified by an image combination scheme* to effect the visual presentation.

Cursor Basic Requirements.

The following is a list of the basic cursor characteristics that should be required on a new image processing display system.

*See GRAPHICS OVERLAYS method of image combination.

3.6 -- Continued.

Programmable Cursor.

Size:	16 x 16 pixels, content programmable by host
Color:	8 including black and white
Position:	Locatable on any pixel of a 1024 x 1024 display (see Trackball). Position writeable by host.
Method of Combination with Imagery:	Programmable between three options: Replacement, Summation, Color Contrast
Method of Combination with Single or Multiple Graphics:	Programmable between two options: *Color Combination*, Hierarchical Override (Cursor has top priority)
Interference:	No noise on video during load or change of position, no interference with video synch.

CURSORS

FEATURE / DISPLAY	PROG. OR FIXED	PROG. SIZE PIXELS	COLOR	NO. OF CURSORS	SCORE							
AYDIN	PROG.	16 X 16	YES	4	7							
COMTAL	PROG.	16 X 16	YES	1	10							
DE ANZA	PROG.; WINDOW	16 X 16	YES	2	7							
GENISCO	FIXED 4 SHAPES	N/A	YES	2	3							
GRINNELL	FIXED 9 X 9	N/A	YES	4	4							
HAZELTINE	FIXED; WINDOW	N/A	NO	2	1							
ISI	FIXED 64 X 64	N/A	NO	1	0							
I^2S	PROG.	64 X 64	YES	1	10							
LEXIDATA	PROG.	10 X 10	YES	1	5							
RAMTEK	PROG.	USES OVERLAY PLANE	YES	8 OTHERS	5							

3.7 Programmable Switching.

Programmable switches are internal circuit devices that provide software or firmware control of the data path through the display system. The switching feature allows the operator to select any one of the loaded refresh memories for display without having to re-write the image to a new memory. Additionally, the data from a refresh memory can be switched selectively to access (or bypass) the black and white and color look-up tables.

The switching can also be used to select any one, all or none of the graphics overlays including the cursor for display. The overlay data may be switched to either access or bypass particular color look-up mappings.

The programmable switch features have been incorporated in all of the display systems under evaluation and are now standard features.

Programmable Switching Basic Requirements.

Refresh Memories:	Selection of any memory for display
Graphics Overlays:	Selection of any overlay for display
Black & White LUT:	Individual selection or de-selection of LUT operation for each refresh memory
	Note: De-selection may be accomplished by a data path around the LUT or by storing the LUT contents and replacing them by the identity function. Selection may be accomplished by again routing the data through the LUT or by restoring the saved LUT contents respectively.

3.7 -- Continued.

Pseudo-Color LUT:	Selection of input from the output of any black and white LUT and/or refresh memory. Note: This may be accomplished without separate, programmably switched data paths by the technique of loading identity functions into the look-up tables provided two capabilities are adhered to: the LUT contents must be saved and replaced by the identity function (or vice versa) within vertical retrace time and 8 bit per color precision must be maintained (N.B. the minimum specified pseudo-color LUT cannot support this).
True Color/ False Color:	Selection of output of any refresh memory to any color
Cursor:	On/Off
Test Patterns:	Selectable on any refresh memory output or not at all
Timing (all switches):	Such that no loss of video synch occurs and that for refresh and graphics switching, stable flicker (for comparative analysis) between memories/overlays is supportable.

PROGRAMMABLE SWITCHES

DISPLAY \ FEATURE	REFRESH CHANNELS	OVERLAY SELECT	B/W LUT SELECT	PSEUDO COLOR SELECT	CURSOR							
AYDIN	YES	YES	YES	YES	YES							
COMTAL	YES	YES	YES	YES	YES							
DE ANZA	YES	YES	YES	YES	YES							
GENISCO	YES	YES (LUT)	YES	YES	YES							
GRINNELL	YES	YES	YES	YES	YES							
HAZELTINE	YES	YES	YES	YES but not independent of B&W	YES							
ISI	YES	YES	YES	YES	YES							
I^2S	YES	YES	YES	YES	YES							
LEXIDATA	YES	YES	YES	YES	YES							
RAMTEK	YES	YES	YES	YES	YES							

3.8 Readback.

The readback feature of a display system enables the host computer to access image data directly from the display refresh memories and the contents of the look-up tables. This capability is critical in displays using a feedback loop or internal microprocessor architecture. In these systems a great deal of high speed, special purpose processing is accomplished to off-load the host computer by performing the processes internal to the display. Since the host CPU was not involved over the processing, it may not be able to recalculate the results and must, therefore, rely on reading the new data back from the display unit.

Most vendors provide readback capability of the refresh memories, the outputs of the color, and black and white look-up tables, the overlay memories and the cursor.

The readback is accomplished by reading the refresh memories and shift registers in the display and writing this data directly into the host CPU memory. From the CPU, the data can be transferred to either disk or tape for archival storage.

The primary uses of the readback feature are listed below:

- Image Archival of Processed Data
- Determine Status of Processing Modules
- Perform Diagnostics on Display System
- Generate Statistics of Processed Data

Readback Basic Requirements and Desirable Features.

3.8.1 Basic Requirements.

The following is a list of the basic readback capabilities that should be incorporated in a state-of-the-art image processing display system capability to read any of the following back to the host:

- Refresh memory contents
- Graphics overlay contents
- Look-up table contents
- Cursor position
- Cursor shape

3.8.2 Desirable Features.

It would be highly desirable to include the status of all display system programmable switches in the readback capabilities of any new display system. This enables host diagnostics to check the operation of programmable switches.

READBACK

FEATURE / DISPLAY	REFRESH	B/W LUTS	CURSOR	PROG. SWITCH STATUS								
AYDIN	YES	YES	YES	YES								
COMTAL	YES	YES	YES	NO								
DE ANZA	YES	YES	YES	YES								
GENISCO	YES	YES	YES	NO								
GRINNELL	YES	YES	YES	NO								
HAZELTINE	YES	NO	NO	NO								
ISI	YES	YES	YES	YES								
I^2S	YES	YES	YES	YES								
LEXIDATA	YES	YES	YES	YES								
RAMTEK	YES	YES	YES	YES								

3.9 Test Patterns.

The test patterns available in most image display systems are used both for monitor calibration and intensity transformation status.

The monitor calibration involves both color gun convergence and display geometry. These conditions are commonly checked using grid or dot patterns. These patterns are displayed to reveal misalignment of the color guns or nonlinearities across the entire monitor screen caused by improper beam deflection.

The intensity transformation status is accomplished using a step wedge (or bar chart) image. The step wedge is usually introduced into the data stream between the image refresh memories and the black and white look-up tables. The wedge is configured to display many pixels of a uniform input intensity in each step. Although the number of steps in the wedge image can vary, the range of step values usually covers the dynamic range of the display (i.e., 0 to 255). Since the pattern can be introduced into any refresh data path, the operator is able to verify the visual effects of any or all of the LUTs. This feature allows the system operator to view the results of gray scale, true color, false color and pseudo-color transformations on known input data.

Test Pattern Basic Requirements.

The following basic test pattern characteristics should be incorporated in any state-of-the-art image processing display system:

There shall be a gray scale bar chart, displayable across the width of the image area (512 pixels) and 10 pixels high. It shall be located at the bottom of the screen and may be within the image

3.9 -- Continued.

area (viz. lines 503 to 512). It shall be inserted into the data stream between the selected refresh memory and its associated black and white look-up table. It shall be programmable to display 64, 128 or 256 grey levels (minimum).

TEST PATTERNS

FEATURE / DISPLAY	GREY SCALE	PSEUDO COLOR	CROSS-HATCH	DOT								
AYDIN	YES	YES	YES	YES								
COMTAL	YES	YES	YES	YES								
DE ANZA	YES	YES	YES	YES								
GENISCO	NO	NO	NO	NO								
GRINNELL	YES	YES	YES	YES								
HAZELTINE	NO	NO	NO	NO								
ISI	YES	YES	YES	YES								
I^2S	NO	NO	NO	NO								
LEXIDATA	YES	YES	YES	YES								
RAMTEK	YES	YES	YES	YES								

3.10 Digital-to-Analog Converters.

Digital-to-Analog Converters (DACs), employed in a display system convert the digital output of the video mixers to analog signals used by the video monitors. The input of the DACs is a serial pixel data stream originating from the display refresh memories. The pixels are formatted in sequential scan lines corresponding to one raster trace on the monitor per scan line. The output data rate from the multiplexer is controlled by the video controller electronics. The Video controller electronics also controls the DAC throughput to provide the necessary sync and blanking for monitor interface.

The DACs are selected to accept a specified digital dynamic range (bits/pixel) and output a conventional 1-Volt range video signal. Typically, image processing displays employ 8-bit DACs thus requiring each of the 256 input levels to be represented in the monitor by approximately 4 mV of the video signal. Many of the systems use smaller 4-bit DACs for pseudo-color operations (see pseudo-color look-up table, Section 6).

Each video channel requires its own DAC (three for color monitors, and one for black and white). Display system vendors currently offer up to 14-bit DAC input and provide up to six DACs per system.

Designing DACs is difficult because of the requirements for high speed and precise analog accuracy. The performance of many existing designs is of poor quality and it is clearly unprofitable to provide 8-bit data handling in refresh memory, LUTs, etc., only to loose the equivalent of two or more bits of precision in the analog video signal. The best display vendors emphasize the care that goes into the design, construction and calibration of the DACs. The performance measures stated below in the requirements are the minimum necessary to provide true performance at the specified precision level.

DAC Basic Requirements.

The following is a list of the basic DAC characteristics that should be met in a state-of-the-art image processing display system:

Number:	3
Precision:	8 bits (minimum)
Performance:	Step increase monotinicity. Step noise less than 1/2 LSB (step height). Glitching--less than 1/2 LSB; less than 1/2 pixel width. Settling time--a guaranteed performance level must be specified.

DIGITAL TO ANALOG CONVERTERS

FEATURE / DISPLAY	NUMBER	WIDTH IN BITS											
AYDIN	≥ 3	8											
COMTAL	3	8											
DE ANZA	3	8											
GENISCO	6	3 x 8 3 x 4											
GRINNELL	3	8											
HAZELTINE	5	8											
ISI	3	14											
I^2S	3	10											
LEXIDATA	4	10											
RAMTEK	4	8											

3.11 Histogram.

The histogram feature in a display system allows the system operator to display a conventional bar chart histogram representing any display image or definable image subset. The histogram is generated in the display hardware and creates little or no overhead burden on the host CPU. The histogram subsystem accesses the pixel data at the output of the look-up tables so that the mappings applied to the image data through the various look-up table transformations are reflected in the histogram. Once the pixel data is accumulated in the subsystem, a standard histogram graph is generated in one of the available graphics overlay memories using the vector generator* module to construct the binary image.

Since the histogram is generated in the graphics overlay, all of the display features and options associated with the graphics memory can be exercised in displaying the histogram or the corresponding image.

The position of the histogram on the display may be controlled by using the cursor to specify the desired position of the graph. The cursor position is used by the histogram subsystem as an address in the graphics overlay for positioning the data.

Histogram Desirable Features.

The following is a list of desirable histogram features that should be incorporated in any state-of-the-art image processing system.

No. of Levels:	256
Calculation Time:	<0.25 secons

*Refer to Subsection 3.15.

3.11 -- Continued.

Area:	Whole screen or subareas defined by irregular polygons, concave or convex, drawn on a selectable graphics overlay by use of the vector generator.
Display:	Selectable display generation at screen location designated by (and subsequently redefinable by) track-ball/cursor control. Display to comprise the conventional bar chart, generated by the vector generator under direct histogram subsystem control into a selectable graphics overlay and with a grey scale wedge inserted into the video underneath the histogram. The wedge is to be inserted prior to the display system look-up tables, thus reflecting the current mapping and relating it directly to the histogram.
Display Sizes:	Selectable between: (a) 128 bins (levels) displayed (b) 256 bins (levels) displayed In either case, display bin width is to be 1 pixel and the display height (bin height) to be 128 pixels.

HISTOGRAM

FEATURE / DISPLAY	NUMBER OF LEVELS	CALCULATION TIME	SUB-AREA CAPABILITY	DISPLAY GENERATION								
AYDIN	N/A	N/A	N/A	N/A								
COMTAL	256	10 sec	NO	YES								
DE ANZA	256	2 FRAMES	YES	YES								
GENISCO	N/A	N/A	N/A	N/A								
GRINNELL	N/A	N/A	N/A	N/A								
HAZELTINE	256	1 FRAME	YES	NO								
ISI	256	10 sec	YES	YES								
I^2S	1024	2 FRAMES	YES	NO								
LEXIDATA	N/A	N/A	N/A	N/A								
RAMTEK	N/A	N/A	N/A	N/A								

3.12 Scroll.

The scroll feature enables the system operator to effect a continuous incremental translation of the display image. The translation can be either up/down or left/right. The scrolling (or panning) is accomplished by indexing a line and/or column to commence each frame in synchrony with the refresh memory. Definition is performed during each vertical retrace period of the monitor. This feature is accomplished independently of the host CPU when the entire image is stored in the display refresh memory. It is also a nondestructive display operation in that the original image data in the refresh mode is not modified. When advanced refresh capability is provided, the operator may pan through a larger image (e.g., 1024 x 1024) at full resolution until the display is centered on a particular point of interest. This type of scroll or pan is usually interactively controlled with a joystick-type device.

A second mode of scrolling occurs when the input image consists of an excess number of scan lines (e.g., an entire flight line of multispectral scanner data). This mode of scrolling requires indexing the refresh memories and writing a new line of pixel data from the host CPU during each refresh cycle. The image appears to move up the screen with the top line of data disappearing and a new line of pixels being added to the bottom at each vertical retrace period. This mode of scrolling is commonly termed "Waterfall". The scrolling motion in this mode can be stopped or continued through the image interactively with keyboard interrupts.

Scroll Feature Basic Requirements.

The following is a list of basic scroll requirements that should be incorporated in any state-of-the-art image processing display system.

3.12 -- Continued.

Direction: Up/Down and Left/Right

Speed: 1 line or column (resp.) per vertical retrace time (minimum)

Performance: Scroll shall be smooth in any of the four directions. When scroll is left or right moving, refresh memory internal multiplexing will give rise to problems and it is acceptable for there to be a displayed image of less than 512 pixels width (e.g., 496 pixels). However, the image which is displayed must scroll by one pixel at a time (i.e., smoothly).

Waterfall: It must be possible to synchronize scroll in any of the four directions with loading of new lines or columns of data. This shall be such that, in up/down scroll, one complete new line of data shall replace the outgoing line per vertical retrace time. The vendor shall specify the rate at which this process can occur in left/right scroll.

SCROLL

FEATURE / DISPLAY	UP-DOWN	LEFT-RIGHT SMOOTH	LEFT-RIGHT JUMP FACTOR IN PIXELS	WATERFALL								
AYDIN	YES	YES	0	YES								
COMTAL	YES	YES	0	YES								
DE ANZA	YES	YES	0	YES								
GENISCO	YES	NO	16	YES								
GRINNELL	YES	YES	0	YES								
HAZELTINE	YES	YES	0	YES								
ISI	YES	N/A	N/A	??								
I^2S	YES	NO	2	YES								
LEXIDATA	YES	YES	0	YES								
RAMTEK	YES	YES	0	YES								

3.13 Zoom.

The zoom feature provides the interactive capability of enlarging subsections of the display image. Zoom is accomplished by specifying the center (in some systems, upper left corner), of the area to be enlarged and an enlargement factor. In most systems the enlargement factor is limited to binary multipliers (i.e., 2, 4, 8, 16). This limitation results from the inherent storage architecture of the refresh memories which permits only binary values of zoom to be easily implemented. Two display vendors offer integer-valued zoom capabilities up to 16X (i.e., 1, 2, 3, ..., 16).

Each scale enlargement is accomplished by using a pixel replication method. With this method, each pixel in the original image is replaced by an array of pixels, all having the same intensity value as the replaced pixel. Using a 2 x 2 array produces a 2-time zoom. The zoom and scroll features can usually be used in conjunction to provide a image pan at the enlarged scale.

Zoom Basic Requirements and Desirable Features.

3.13.1 Basic Requirements.

The following is a list of the basic zoom requirements that should be incorporated in any state-of-the-art image processing display system:

Technique: Pixel replication

Ratios: 2, 4, 8:1 (minimum)

Aspect Ratio: 1:1

3.13.1 -- Continued.

Location: The zoomed subarea shall be programmably locatable anywhere within the unzoomed 512 x 512 pixel space, i.e., down to the single pixel level. The subarea must be redefinable during each vertical retrace time thus a smooth pan feature is achievable.

Operating Mode: Black and white and color (true, false or pseudo)

3.13.2 Desirable Features.

Integer valued zoom would be a desirable attribute to the display system providing a minimum zoom range of 1:1 to 1:6.

ZOOM

FEATURE / DISPLAY	PIXEL REPLICATION	BINARY	INTEGER	INTERPOLATION	PAN						
AYDIN	YES	2, 4, 8, 16	NO	NO	YES						
COMTAL	NO	NO	NO	NO	NO						
DE ANZA	YES	2, 4, 8	NO	NO	YES						
GENISCO	YES	YES 2, 4, 8	NO	NO	YES						
GRINNELL	YES	YES 2, 4, 8	NO	NO	16 x 16 LOC.						
HAZELTINE	NO	NO	NO	NO	NO						
ISI	YES	YES	1-16	NO	YES						
I^2S	YES	2, 4, 8	NO	NO	YES 1 x 2						
LEXIDATA	YES	2, 4, 8	NO	NO	YES						
RAMTEK	YES	YES	1-16	NO	YES						

3.14 Split Screen.

The split screen display feature provides a means of viewing portions of two images simultaneously. The system operator is permitted to read subsets of image data from any two refresh memories and displays one adjacent to the other in either a left/right or top/bottom orientation. This feature is commonly used to evaluate the results of image processing operations, to observe differences between various channels of multispectral imagery and to observe effects of time in multitemporal imagery.

The display of the split screen data is achieved interactively by specifying the desired subset of each of the two image files to be displayed. The split screen mode module then, in conjunction with the scroll module, based on the split orientation, determines the refresh access sequence that will serially provide the desired visual effect in the resulting full raster presentation.

Split Screen Basic Requirements and Desirable Features.

3.14.1 Basic Requirements.

Orientation: Left half/right half
Top half/bottom half

Operation: In conjunction with scroll such that any contiguous 256 columns or rows may be specified from any two refresh memories and displayed on the left half and right half or top half and bottom half of the screen, respectively (mosaicing).

3.14.2 Desirable Features.

It would be desirable to incorporate the left/right and top/bottom split screen features simultaneously to result in a four quadrant mosaic reading four refresh memories to provide up to four independent sets of data for observation. This feature is also available for a four way split into nonequal rectangular areas (such as may be defined by positioning a full screen crosshair).

SPLIT SCREEN

FEATURE / DISPLAY	LEFT-RIGHT	TOP-BOTTOM	4-QUADRANT MOSAICING									
AYDIN	YES	YES	YES									
COMTAL	YES	YES	NO									
DE ANZA	YES	YES	YES									
GENISCO	NO	NO	NO									
GRINNELL	YES	YES	NO									
HAZELTINE	YES	YES	YES									
ISI	NO	YES	NO									
I^2S	YES	YES	YES									
LEXIDATA	YES	NO	NO									
RAMTEK	YES	YES	YES									

3.15 Vector Generator.

The vector generator module is used to create all of the line and curve data in the graphics overlays. This unit can be controlled, through the graphic subsystem, by either the host computer or by a microprocessor in the display system. Each graphic is produced by generating a vector to represent each line segment to be displayed in the graphic overlay. The parameters for each segment are fed to the vector generator (i.e., start point, end point and line function). The algorithm is calculated in hardware and the appropriate pixels are written into the graphics refresh memory.

The shape and scale of the resultant graphic are determined by the line function parameters which are commonly generated by the Arithmetic Logic Unit (ALU). The positioning parameters, the start and end points, are often interactively generated using the cursor or keyboard to identify positional origins or junction points along an irregular boundry.

Parameters for frequently used graphics such as cursors, histogram and function graphics, and image boundry lines are stored in the display memory for direct access by the vector generator.

The output of the vector generator is the X,Y address in the graphic refresh for each pixel that is to be "turned on" to generate the overlay image.

Although all of the vendors evaluated in this report provide a straight line generator, only a few have the capability of generating a curved segment between two end points. Most of the vendors provide the capability of generating random vectors using serial data stream interactive devices (i.e., trackball or joystick).

3.15 -- Continued.

It should be noted here that in the course of the display study no attempt was made to approach state-of-the-art technology in the graphics capabilities available outside of the image processing display oriented vendors. And, that a high level of sophistication has been achieved that has not been incorporated into image processing display systems.

Vector Generator Basic Requirements.

The following is a list of basic vector generator characteristics that should be incorporated in a new state-of-the-art image processing display system.

Type:	Straight lines
Operation:	Into selectable graphics overlay
Speed:	$\leq$ 50 μs per point

VECTOR GENERATION

FEATURE / DISPLAY	HARDWARE	FIRMWARE	STRAIGHT LINE	CURVES	RANDOM (VIA TRACK BALL, JOYSTICK)							
AYDIN	YES	YES	YES	YES	YES							
COMTAL	N/A	YES	YES	NO	YES							
DE ANZA	YES	YES	YES	NO	YES							
GENISCO	YES	YES	YES	NO	YES							
GRINNELL	YES	N/A	YES	NO	YES							
HAZELTINE	N/A	N/A	N/A	N/A	N/A							
ISI	N/A	YES	YES	YES	YES							
I^2S	YES	NO	YES	NO	NO							
LEXIDATA	N/A	YES	YES	CIRCLES	YES							
RAMTEK	N/A	YES	YES	YES	YES							

3.16 Character Generator.

The character generator module provides the conversion of character string data to alphanumeric display of text on the display monitor. This feature is used primarily for image annotation and is facilitated using the graphics overlay memory of the display system.

The character generator translates ASCII (8-bit) input into a programmable read-only memory (PROM) address which contains a binary array representing the shape of the corresponding alphanumeric character. The character array is then written in a selected graphic overlay memory at a predetermined address in the overlay. The graphic overlay may be addressed in blocks by the character generator for standard character and line spacing, however, several vendors produce display systems that permit random positioning of characters in the graphics overlay.

The currently available display systems use either hardware character generators or microprocessor controlled character generators. Several of the firmware controlled character generators use PROM as a character look-up table making the font and character style programmable. The number of characters available in these systems range between 64 and 128.

Character Generator Basic Requirements.

The following is a list of basic character generator features that should be incorporated in state-of-the-art image processing display system.

3.16 -- Continued.

Operation:	Into selectable graphics overlays
No. of Characters:	64 (minimum)
Character Host:	5 x 7, 10 x 14
Location:	On any pixel (alphanumeric format such as 80 x 25 is unacceptable).

CHARACTER GENERATION

FEATURE / DISPLAY	HARDWARE	FIRMWARE	#FONTS	ALPHA-NUMERIC FORMAT	RANDOM LOCATION	NUMBER OF CHARACTERS						
AYDIN	YES	YES	3 PROG.	PROG.	YES	64						
COMTAL	N/A	YES	1	NO	YES	64						
DE ANZA	YES	YES	PROG.	NO	YES	64						
GENISCO	YES	YES	1	NO	YES	96 128 OPT.						
GRINNELL	YES	N/A	4	NO	YES	64 128 OPT.						
HAZELTINE	N/A	N/A	N/A	N/A	N/A	N/A						
ISI	N/A	YES	1	YES	NO	64						
I^2S	OPT.	YES	PROG.	NO	YES	PROG.						
LEXIDATA	N/A	YES	PROG.	NO	YES	ANY NO.						
RAMTEK	YES	YES	PROG.	NO	YES	128						

3.17 Image Combination.

The image combination feature permits the display system operator to perform arithmetic operations on multiple image data. These arithmetic operators are:

- Add
- Subtract
- Multiply
- Divide.

The operations are performed by specifying the refresh memory of each input image and the order of the operation. The result of these operations is an output image in which each pixel intensity value reflects the arithmetic operation on the corresponding pixels of the input images.

Image combination operations are commonly used with multispectral and multitemporal data where multiple images exist that are registered to one another on a pixel by pixel basis. The coincident ground cover permits change detection to be accomplished by subtracting images acquired at different times, and spectral signature enhancement by taking the ratio (divide) of two bands of multispectral imagery.

There are several methods of performing these operations:

Software

Image combinations in software typically are accomplished with the image data residing on a disk memory. The input images are read into the CPU a line at a time where the arithmetic operation is performed a pixel at a time. The results are then passed back to the

3.17 -- Continued.

disk creating an output image file. The output image is subsequently scaled to the appropriate intensity range for display on the monitor. This mode is very slow, but easily achieved on any host Arithmetic Logic Unit (ALU).

Firmware

Image combinations are performed under microprocessor control using programmed read and write instruction sets between the refresh memories, adder arrays, look-up tables and shift registers. The resulting image is written to an available refresh memory and is then immediately available for display on the following refresh cycle. Once the processing is initiated no interaction is required with the host CPU.

Hardware

Hardware combination operations are performed at extremely high rates using programmable switches to establish the data path through the required modules to perform the intended operation. The result is scaled on line and displayed in real or near real time.

The scaling function is required in these arithmetic combinations because the operations produce output images with intensity ranges beyond the range of either of the input images.

Using two 8-bit input images the following results could potentially be achieved with the four arithmetic operations

3.17 -- Continued.

Operation	Input Levels Range	Output Range	Required Scaling Factor
Add	0,255	0,510	2:1
Subtract	0,255	-255,255	2:1
Multiply	0,255	0,65025	256:1
Divide	0,255	0,255 (+ Rationals)	256:1

Image Combination Basic Requirements.

The follow is a list of the basic image combination features that should be incorporated in a state-of-the-art image processing display system.

Real time: Addition and subtraction of two or more images, maintaining precision of the result up to 16 bits

Near Real Time: 16 bit accuracy multiplication and division of two or more images in less than 0.5 seconds.

Rescaling: Means must be provided to reduce precision of a computed result to 8 bits for display.

IMAGE COMBINATION

FEATURE / DISPLAY	REAL TIME ADD, SUBT MULT, DIV	PRECISION BITS	NUMBER OF REAL-TIME PASSES TO ADD/SUBT	NUMBER OF REAL-TIME PASSES TO MULT	NUMBER OF REAL-TIME PASSES TO DIV	WHILE LOADING						
AYDIN	N/A	N/A	N/A	N/A	N/A	N/A						
COMTAL	N/A	N/A	N/A	N/A	N/A	YES FOR DIGITIZER						
DE ANZA	YES	DUAL 16	1	9	17	YES FOR DIGITIZER						
GENISCO	N/A	N/A	N/A	N/A	N/A	N/A						
GRINNELL	N/A	N/A	N/A	N/A	N/A	YES FOR DIGITIZER						
HAZELTINE	N/A	N/A	N/A	N/A	N/A	N/A						
ISI	N/A	N/A	NA	N/A	N/A	YES FOR DIGITIZER						
I^2S	YES	13	1	N/A APPROX BY LUT	N/A APPROX. BY LUT	YES FOR DIGITIZER						
LEXIDATA	N/A	N/A	N/A	N/A	N/A	N/A						
RAMTEK	N/A	N/A	N/A	N/A	N/A	N/A						

3.18 Feedback Loop.

The feedback loop feature provides a data path from the output of refresh memory through an internal processing pipeline, back to the refresh memory. This feature establishes the capability to perform sophisticated iterative and spatial processing functions. The feedback loop coupled with single memory cycle rates for refresh, intensity transformation, look-up table load and four direction scrolling enables multiple pass processing to be accomplished in times measured in image refresh cycles.

Some of the functions that can be performed on image data using this feature are:

- First derivitive images
- Gradient images
- Spatially filtered images
- Multiple image averages
- Angle dependent radiance

The feedback loop has been incorporated in only two of the systems evaluated under the display study and, although the data path is identical in both systems, the primary purpose for the feature is altogether different between the two.

One system uses the loop to write the processed data back to the refresh where it can be accessed by the host computer for archive and statistics generation. The other system uses the loop primarily for iterative and spatial processing. The result is that both can perform the same operations. However, the design of the arithmetic processor on the former unit which uses log/antilog look-up tables for multiplication operations compounds the error of approximation on each iteration of processing. This points out the sensitivity of the design specifications for this feature.

3.18 -- Continued.

Feedback Loop Basic Requirements.

The following is a list of the basic feedback loop features that should be incorporated in a state-of-the-art image display system.

Width:	16 bits
Input/Output:	Any refresh channel for either feedback byte
Scroll:	Must operate in conjunction with scrolled memories
Processing:	Matrix multiply and add, divide and subtract, with two images, or an image and a coefficient-matrix. Neighboring pixel arithmetic and logical operations.

FEEDBACK LOOP

FEATURE / DISPLAY	WIDTH BITS	SELECTABLE REFRESH CHANNEL INPUT	SELECTABLE REFRESH CHANNEL OUTPUT	RETAIN PRECISION								
AYDIN	N/A	N/A	N/A	N/A								
COMTAL	N/A	N/A	N/A	N/A								
DE ANZA	DUAL 16	YES	YES	YES								
GENISCO	N/A	N/A	N/A	N/A								
GRINNELL	N/A	N/A	N/A	N/A								
HAZELTINE	8	YES	YES	NO								
ISI	N/A	N/A	N/A	N/A								
I^2S	13	YES	YES ONLY ONE 13 BIT O/P	YES ON ONE CHANNEL								
LEXIDATA	N/A	N/A	N/A	N/A								
RAMTEK	N/A	N/A	N/A	N/A								

3.19 Internal Processing.

A display system containing internal intelligence has more inherent power and flexibility than the traditional display systems of the past which were normally all hardwired. There are three different kinds of internal intelligence encountered in the display systems evaluated (Hazeltine and Grinnell support no internal intelligence):

- Feedback-loop and real-time image combination
- Microprocessor used only for display system control
- Microprocessor used both for display control and processing operations.

Feedback-loop and real-time image combination are treated elsewhere in this report. The other two kinds both involve the integration of a microprocessor into the display system. The microprocessor chosen varied from off-the-shelf microprocessors to a unit designed and built from scratch by the display vendor. LEXIDATA was the only vendor that used their microprocessor for control only, i.e., the microprocessor could not access data in the refresh channel or graphic overlays. All the other vendors using microprocessors provided for access to the refresh channels and graphic overlays. In these systems, the microprocessor can perform most operations that a host CPU could perform, thus off-loading the processing burden from the host. The limitations being the volume of machine instructions which can reside in the microprocessor's memory, and for some operations slower processing rate. These limitations are offset by reducing the processing and I/O burden on the host CPU. Additionally, a library of microprocessor operations can be maintained on the host's disk and down-loaded to the internal microprocessor as needed.

3.19 -- Continued.

One final advantage of a display system containing a microprocessor is that, given the approximate diagnostics written for the microprocessor, the microprocessor can isolate display system problems to the board level; thus, greatly reducing the effort and time necessary to maintain the display system.

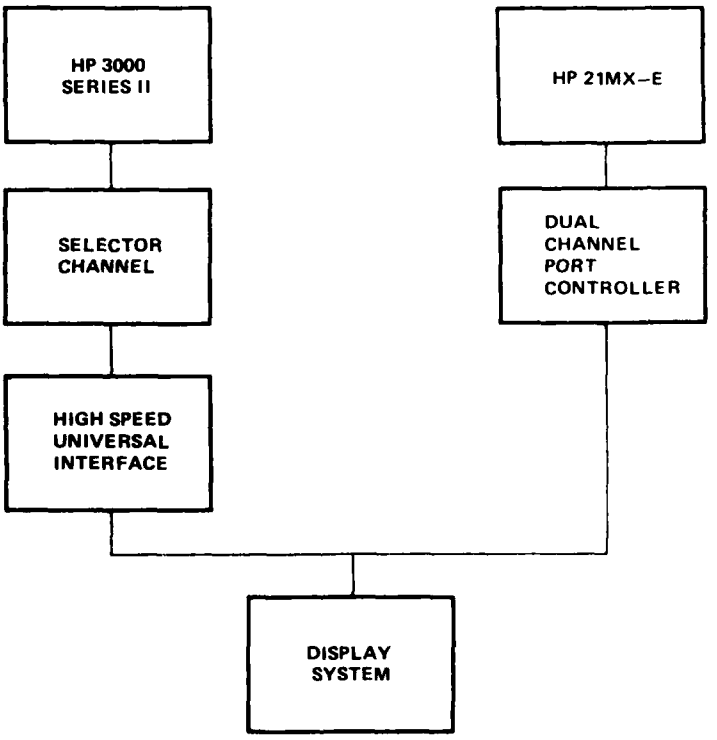
All of the microprocessors used in the display systems were reasonably equivalent. The major difference being the technique used to integrate the microprocessor into the display system.

INTERNAL PROCESSING

DISPLAY \ FEATURE	MICRO-PROCESSOR											
AYDIN	8086											
COMTAL	LSI-11											
DE ANZA	LSI-11											
GENISCO	OWN											
GRINNELL	NO											
HAZELTINE	NO											
ISI	LSI-11											
I^2S	8080											
LEXIDATA	OWN											
RAMTEK	Z80 & 2901											

3.20 Host Interface.

The host interface provides both a control point and a data path between the host CPU and the display system. All display vendors were evaluated with respect to the following hardware configuration:



As can be seen, the display system is dual-ported between two host CPUs, the HP3000 Series II and the HP21MX-E computers. The major requirement of the interface is to make control and data transfer to and from the host as clean, easy and fast as possible.

3.20 -- Continued.

Host Interface Basic Requirements.

Features: When one port is in use, the other port must appear busy to its respective host computer.

Image data or graphic overlay data may be loaded or read at any time without interference to refresh (noise or loss of synch).

LUT contents and cursor shape definitions will be loaded only during vertical retrace periods. The interface will handle this without requiring the host to verify under software control that the display is in fact in the vertical retrace area before issuing the output operation.

Rectangular portions of the refresh memories should be loadable without physically addressing each line (i.e., auto address increment mode).

Any desired refresh memory (image or graphic plane) may be set to zero by sending a sequence of control and data words that is less than 100 words long (i.e., mass erase command).

Sufficient growth capability should exist in the control definition scheme that additional refresh memories or other new features may be

3.20 -- Continued.

added to a display subsystem without necessitating re-definition of the existing control definition.

All features at the display must be accessible through the interface from the host.

If the display contains a microprocessor, code for it must be down-loadable through the interface.

The ability to execute a master reset on both the interface and the display system.

Speed: The interface will maintain a transfer rate which corresponds to the minimum of the host interface and the display sustainable transfer rates.

INTERFACE

FEATURE / DISPLAY	HP3000	HP21MX	BURST TRANSFER RATE (PIXELS/SEC)	BLOCK TRANSFER RATE (PIXELS/SEC) (RFM)	BLOCK TRANSFER RATE (PIXELS/SEC) (OVERLAYS)	BLOCK TRANSFER RATE (ELEMENTS/SEC) (LUTS)	SYNCH WITH VERTICAL RETRACE FOR LUT LOAD?	AUTO ADDRESS INCREMENT?				
AYDIN	NO	NO	1.25M	625K	625K	1.25M	YES	YES				
COMTAL	YES	YES	850K	850K	6.8M	850K	YES	YES				
DE ANZA	YES	YES	1.6M	1.6M	12.8M	1.6M	YES	YES				
GENISCO	NO	NO	400K	400K	3.2M	333K	NO	YES				
GRINNELL	NO	YES	666K	666K	666K	2M	YES	YES				
HAZELTINE	NO	NO	666K	666K	1.3M	??	YES	NO				
ISI	NO	YES	2M	1M	8M	??	??	YES				
I^2S	YES	YES	2M	1M	8M	1M	YES	YES				
LEXIDATA	NO	NO	2M	2M	2M	??	YES	YES				
RAMTEK	NO	YES	900K	900K	900K	??	YES	YES				

INTERFACES

FEATURE / DISPLAY	DMA	DIRECT I/O	READY/NOT READY SIGNAL	POWER ON IN KNOWN STATE?	#BYTES REQ'D TO CLEAR REFRESH CHANNEL	MICRO PROCESSOR DOWN – LOADABLE?	HP INTERFACE CHECK IN-PLANT?					
AYDIN	YES	NO	YES	YES	<10	YES	SIMULATOR					
COMTAL	YES	NO	NO	NO	.25M	YES	NO					
DE ANZA	YES	YES	YES	YES	<10	N/A	SIMULATOR					
GENISCO	YES	YES	YES	NO	<10	YES	SIMULATOR					
GRINNELL	NO	YES	YES	YES	<10	N/A	SIMULATOR					
HAZELTINE	YES	NO	YES	NO	.25M	N/A	SIMULATOR					
ISI	YES	YES	YES	NO	<10	NO	NO					
I^2S	YES	NO	YES	NO	<30	??	YES					
LEXIDATA	YES	YES	YES	NO	<10	YES	NO					
RAMTEK	NO	YES	YES	YES	<10	YES	NO					

4. SUMMARY.

4.1 Trends.

The aforementioned improvements in hardware and application of system design philosophies is leading to far more powerful displays at no increase in cost and with reduction in overall system size. In fact, the continued downward trend in memory cost may bring system cost reductions since memory is such a major portion of a system. The following trends are particularly important.

Better system design is allowing greater modularity, more flexibility and programmability and inherently allowing for future growth in both capability and size. It should be anticipated that bus-oriented architectures will become standard for this reason, but at current technology levels, refresh rates are too high for the bus concept to extend to that part of the system. Correspondingly, feedback loops will remain hard-wired although of course they may be incorporated in otherwise bus-oriented architectures.

Significant changes in refresh memories are already apparent and such trends as programmability and dual use for processing will intensify. The speed of refresh memories will continue to improve both in terms of external I/O rates (such as to refresh 1K x 1K pixel displays) and internally, through future chip cycle times, to allow less multiplexing and hence more random access for processing. In conjunction with monitor advances, refresh memories will in future support 1K x 1K pixel displays, 60 frames per second noninterlaced operation and programmable display format presentation. (Some of these features are already in production though not all on any one system.) Auxiliary use of refresh memory as fast processing memory will become much more widespread as memory design, memory cost and systems architectural advances combine to make it an efficient use of resources to perform the processing in the memory.

4.1 -- Continued.

A clear trend in the systems is the incorporation of internal intelligence. Currently this covers the gamut from custom designed microprocessors for control, to powerful miniprocessors for both control and internal processing. It is anticipated that intelligence will become further distributed with control, processing, man-machine interface, and mass data I/O (directly between the display and disk) being performed by dedicated processors. As such, the systems will be more stand-alone and the duties of a host computer will diminish -- perhaps to just data base management.

4.2 Vendor Capabilities.

This section will make brief summary comment on each vendor to assist identification of the strength in application area of the vendor.

4.2.1 Aydin.

Excellent bus-oriented, modular architecture. Slow internal processing in integrated microprocessor. Excellent growth potential for general application.

4.2.2 Comtal.

Inflexible system -- no architecture per se. Moderate internal processing in integrated L.S.I.-11. Poor growth potential. General application.

4.2.3 DeAnza.

Somewhat inflexible architecture. Very sophisticated near-real time processing plus moderate processing in integrated L.S.I.-11. Excellent growth potential with application to advanced rapid analysis.

4.2.4 Genisco.

Reasonable architecture but not strongly oriented to multiple grey shade imagery. Slow internal processing in integrated microprocessor. Application to graphics oriented applications.

4.2.5 Grinnell.

Inflexible architecture and no internal processing. No growth potential. Best for simple, low cost application.

4.2.6 Hazeltine.

No production units hence an architecture intended for one application (earth resources). Poor growth potential.

4.2.7 I^2S.

Good architecture especially for many image, color application. Real and near real time processing in hardware plus microprocessor control. Moderate growth potential. Excellent for multispectral data applications.

4.2.8 ISI.

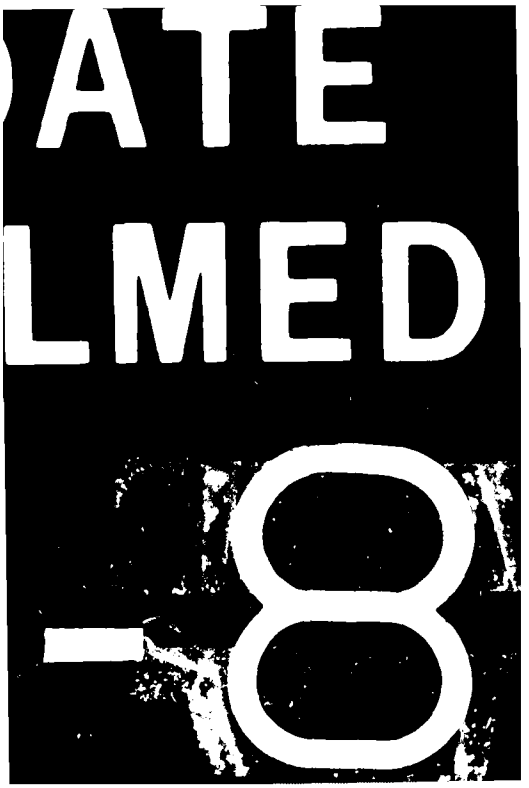
Excellent bus-oriented architecture with programmable refresh memory and moderate internal processing. Good growth potential for all applications.

4.2.9 Lexidata.

Excellent architecture with programmable refresh memory. No internal processing. Custom integrated microprocessor for very flexible internal control. Excellent growth potential for all applications.

4.2.10 Ramtek.

Oriented almost exclusively to graphics applications, but very considerable potential for future should serious efforts be made to handle multiple-grey shade data. Highly flexible internal microprocessor control.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